What is claimed:

SUB B1

1. A method for manufacturing a semiconductor device having a trench isolation region, the method comprising the steps of:

(a) forming a trench in a semiconductor layer;

(b) forming a dielectric layer that fills the trench; and

(c) conducting a thermal treatment of the dielectric layer, wherein the thermal treatment is conducted at temperatures of at least 1050°C.

C1

2. A method for manufacturing a semiconductor device having a trench isolation region according to claim 1, wherein, in the step (b), the dielectric layer is formed with a film density of at least 2.1g/cm^3.

3. A method for manufacturing a semiconductor device having a trench isolation region according to claim 1, wherein the temperature of the thermal treatment is 1100°C or higher.

4. A method for manufacturing a semiconductor device having a trench isolation region according to claim 1, wherein the temperature of the thermal treatment is in the range of 1050°C to 1250°C.

5. A method for manufacturing a semiconductor device having a trench isolation region according to claim 1, wherein the dielectric layer is formed by a high density plasma CVD method.

6. A method for manufacturing a semiconductor device having a trench isolation region according to claim 1, further comprising the step (d) of forming a well in the semiconductor layer, and the step (c) is conducted before the step (d).

B

SUB B2

7. A method for manufacturing a semiconductor device having a trench isolation region according to claim 1, wherein the trench includes sidewall surfaces and a bottom surface, the method further comprising of thermally oxidizing the sidewall surfaces and the bottom surface of the trench.

8. A method for manufacturing a semiconductor device having a trench isolation region according to claim 7, wherein the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 700°C to 1150°C.

C1

9. A method for manufacturing a semiconductor device having a trench isolation region according to claim 7, wherein the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 950 to 1150°C.

10. A method for manufacturing a semiconductor device having a trench isolation region according to claim 7, wherein the thermally oxidizing the sidewall surfaces and the bottom surface yields an oxidation layer having a thickness in the range of 10 nm to 100 nm.

11. A method for manufacturing a semiconductor device having a trench isolation region according to claim 1, wherein the semiconductor layer comprises an epitaxial growth layer formed on a semiconductor substrate.

12. A method for manufacturing a semiconductor device having a trench isolation region according to claim 11, wherein the epitaxial growth layer has a thickness of at least 2 μm.

C1

13. A method for manufacturing a semiconductor device having a trench isolation region according to claim 1, wherein the trench is formed with a trench width of no greater than 0.35 μm.

SUB B3

14. A method for manufacturing a semiconductor device having a trench isolation region, the method comprising:

forming a trench in a semiconductor layer;

forming a dielectric layer in the trench; and

heating the dielectric layer at a temperature of at least 1050°C.

15. A method as in claim 14, wherein the trench includes sidewalls and a bottom surface, the method further comprising:

forming a trench oxide layer on the sidewalls and bottom of the trench prior to forming the dielectric layer in the trench.

C1

16. A method as in claim 15, wherein the trench oxide layer is formed by oxidizing the sidewalls and bottom surface, and the trench oxide layer is formed to have a thickness in the range of 10 nm to 100 nm.

17. A method as in claim 14, wherein the heating the dielectric layer is carried out for a time in the range of 20 minutes to 120 minutes at a temperature in the range of 1050°C to 1200°C.

18. A method as in claim 14, further comprising forming at least one transistor adjacent to the trench isolation region, the at least one transistor being formed after heating the dielectric layer at a temperature of at least 1050°C.

Sub B4

19. A method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

forming a first layer on a semiconductor substrate;

forming a polishing stopper layer above the first layer;

forming at least one trench by etching the first layer while using the polishing stopper layer as a mask;

forming a dielectric layer in and above the trench; and

planarizing the dielectric layer using the polishing stopper layer as a stopper.

20. A method as in claim 19, wherein the first layer comprises an epitaxial growth layer.

21. A method as in claim 19, further comprising removing the polishing stopper layer after planarizing the dielectric layer.

C1

22. A method as in claim 19, further comprising oxidizing at least a portion of the first layer in the at least one trench prior to forming the dielectric layer in and above the trench.

23. A method as in claim 22, further comprising forming a pad layer between the first layer and the polishing stopper layer.

24. A method as in claim 21, further comprising subjecting the dielectric layer to a thermal treatment at a temperature of at least 1050°C after removing the polishing stopper layer.

25. A method as in claim 24, wherein the thermal treatment is carried out in an atmosphere comprising 0.1 volume % to 10 volume % oxygen.

Subt a'

26. A method as in claim , wherein the dielectric layer is formed using high density plasma chemical vapor deposition.

27. A semiconductor device including a trench isolation region and transistor element regions, comprising:

a semiconductor substrate;

a first layer formed on the semiconductor substrate;

a trench isolation region formed in the first layer; the trench isolation region including a oxide layer and a dielectric material layer therein; and

transistor element regions separated by the trench isolation region.

28. A device as in claim 27, wherein the first layer comprises an epitaxial growth layer.

29. A device as in claim 27, wherein the dielectric material layer comprises a material having a density of at least 2.1g/cm^3.

30. A device as in claim 27, wherein the dielectric material layer comprises a material having a density of at least 2.3g/cm^3.

31. A semiconductor device including a trench isolation region, comprising:

a semiconductor substrate;

an epitaxial growth layer on the semiconductor substrate;

a trench provided in the epitaxial growth layer;

an annealed dielectric layer in the trench;

a trench oxide film formed between the epitaxial growth layer and the dielectric layer; and

transistor element regions separated by the trench isolation region.

B

ADD B5